In the Claims

47. (Previously amended) An integrated circuit comprising:

a semiconductive substrate;

a layer comprising copper over the substrate;

a layer of intermetallic material within the layer comprising copper, the intermetallic material layer comprising copper and palladium and having a thickness of from about 50 to about 150 Angstroms; and

a conductive connection on the intermetallic layer.

48. (Previously amended) The integrated circuit of claim 47 wherein the intermetallic material consists of an intermetallic.

49. (Previously amended) The integrated circuit of claim 47 wherein the intermetallic material is less susceptible to formation of metal oxide compared to copper.

50. (Previously amended) The integrated circuit of claim 47 wherein the layer comprising copper consists of copper aside from the intermetallic material layer.

51. (Previously amended) The integrated circuit of claim 47 wherein the intermetallic material consists of copper and palladium.

52. (Cancelled)

53. (Previously amended) The integrated circuit of claim 47 wherein about 150 Angstroms of the layer comprising copper is intermetallic material.

54. (Original) The integrated circuit of claim 47 wherein the conductive connection comprises an integrated circuit via or an integrated circuit wire bond.

55. (Currently amended) An integrated circuit comprising:

a semiconductive substrate;

a layer comprising ~~Cu~~ Al over the substrate;

a layer of alloy material within the layer comprising ~~Cu~~ Al, the alloy material layer comprising intermetallic ~~Cu_3Pd~~ Al-Pd ~~and having a thickness of from about 50 to about 150 Angstroms~~; and

a conductive connection on the alloy layer.

56. (Currently amended) The integrated circuit of claim 55 wherein the alloy material consists of ~~Cu_3Pd~~ intermetallic Al-Pd.

57. (Currently amended) The integrated circuit of claim 55 wherein from about 50 to about 150 Angstroms of the layer comprising ~~Cu~~ Al is alloy material.

58. (Previously added) The integrated circuit of claim 55 wherein the conductive connection comprises an integrated circuit via or an integrated circuit wire bond.

59. (Previously amended) An integrated circuit comprising:

a semiconductive substrate;

a layer consisting of copper over the substrate;

a layer of intermetallic material over the copper layer, the intermetallic material layer consisting of copper and palladium and having a thickness of from about 50 to about 150 Angstroms; and

a conductive connection on the intermetallic layer.

60. (new) The integrated circuit of claim 47 wherein the thickness of the intermetallic material layer is sufficient to reduce oxidation of the layer comprising copper.

61. (new) The integrated circuit of claim 55 wherein a thickness of the alloy material layer is sufficient to reduce oxidation of the layer comprising Al.

62. (new) The integrated circuit of claim 59 wherein the thickness of the intermetallic material layer is sufficient to reduce oxidation of the layer consisting of copper.